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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/698,531	11/03/2003	Yong-Nien Rao	RAOY3001/EM	1415

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EXAMINER

NGUYEN, JIMMY H

ART UNIT	PAPER NUMBER
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2629

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/698,531

Applicant(s)

RAO ET AL.

Examiner

Jimmy H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 and 8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/23/2007 has been entered. Claims 1-5 and 8 are currently pending in the application. An action follows below:

Notice to Applicants

2. Examiner reminds the Applicants that when there is any amendment to a claim, a listing of all claims including **cancelled claims** must be presented in compliance with the Revised Amendment Practice 37 CFR 1.121. In the amendment submitted with the RCE filed on 1/23/2007, the listing of claims does not include cancelled claims 6, 7 and 9.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-5 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

As to claims above, the disclosure, when filed, does not fairly convey to one of ordinary skill in the art that applicants had in their possession the claimed limitations, “a polarity arrangement timing generator (PATG) for generating a polarity arrangement control (PAC) signal from a plurality of predefined polarity arrangement control signals” in lines 7-10 of independent claim 1 and “a timing generation step for generating a polarity arrangement control (PAC) signal from a plurality of predefined polarity arrangement control signals” in lines 4-6 of independent claim 8. The specification, especially the last paragraph on page 5 (as pointed out by the Applicants; see last paragraph on page 5 of the amendment), merely discusses all the elements of the PAPDD, but not the PATG, and discloses “polarity arrangement control signals sent from the PATG 320” (see lines 19-21 on page 5 of the specification). There is nowhere in the original disclosure to disclose a polarity arrangement timing generator (PATG) **generating** a polarity arrangement control (PAC) signal **from** a plurality of predefined polarity arrangement control signals, as presently claimed.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 2, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Onoya (US 2001/0034075 A1).

As to these claims, the claimed invention reads on the Onoya reference as follows: Onoya discloses a liquid crystal display (LCD) device and an associate driving method for controlling

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the polarity of the LCD panel, the LCD device (see Fig. 12) comprising a LCD panel (413) having plurality of pixels (415); a scanning unit (409) connected to the display panel by a plurality of scanning lines (410) so that the scanning unit controls the pixels of the display panel via the scanning lines; a polarity arrangement timing generator (PATG) (a circuitry including elements 201, 203, 207 and 208, see Fig. 8) for generating a plurality of polarity arrangement control (PAC) signals for a plurality of frames (polarity data signal; see Figs. 4 and 8), each corresponding to a set of aperiodical polarity order (see Fig. 4 which shows each of five PAC signals corresponding to a set of aperiodical polarity order); and a polarity arrangement programmable data driver (PAPDD) (a circuitry including elements 205, 206, and 412; see Figs. 8 and 12) connected to a plurality of data lines (408) and receiving the polarity arrangement control signals so as to output a set of aperiodic polarity order to the data lines so that the polarities of the pixels are distributed aperiodically (see Figs. 4 and 7). Onaya further teaches the PAPDD (205, 206, 412) including a plurality of sampling/hold registers (registers 401 and latches 403 and 404, see Fig. 12) for latching digital signals sent to the pixels of the display panel (paragraph 0318). As shown in Fig. 4, Onaya teaches that when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the first frame opposite to the polarity of the second frame, the polarity of the third frame opposite to the polarity of the fourth frame, and etc., i.e., the polarity of the odd frame opposite to the polarity of the even frame. In other words, Onaya teaches that when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the half (odd) of the frames opposite to the polarity of the other half (even) of the frames, such that the polarity distribution of the one half of the frames is

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complementary to that of the other half of the frames. Accordingly, all the limitations of these claims are read in the Onoya reference.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,335,721 B1) hereinafter Jeong721 and further in view of Onoya.

As to claims 1 and 8, the claimed invention reads on the Jeong721 reference as follows: Jeong721 discloses a liquid crystal display (LCD) (see col. 1, line 12) and an associate driving method for controlling the polarity of the LCD panel, the LCD device comprising a LCD panel (col. 1, line 33) having a plurality of inherent pixels; a scanning unit (a gate driver, col. 5, line 13) connected to the display panel by a plurality of scanning lines so that the scanning unit controls the pixels of the display panel via the scanning lines; a polarity arrangement timing generator (PATG) (an inherent circuitry for providing a plurality of control signals such as and video signals to the source driver, see Fig. 4) for generating a plurality of polarity arrangement control (PAC) signals (POL_INT; see Fig. 4) for a plurality of frames, each corresponding to a set of polarity order; and a polarity arrangement programmable data driver (PAPDD) (a LCD source driver as shown in Fig. 4) connected to a plurality of inherent data lines and receiving the polarity arrangement control signals (POL_INT, CLK1, CLK2, LATCH_OE signals, see Fig. 4) so as to output a set of polarity order to the data lines (see Figs. 6A and 6B). Accordingly,

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Jeong721 discloses all the claimed limitations of these claims except that Jeong does not expressly disclose that the PAPDD outputs a set of **aperiodic** polarity order to the data lines so that the polarities of the pixels are distributed aperiodically; and when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the half of the frames opposite to the polarity of the other half of the frames, such that the polarity distribution of the one half of the frames is complementary to that of the other half of the frames, as presently recited in claims 1 and 8.

However, Onoya discloses a related LCD device comprising a PATG (a circuitry including elements 201, 203, 207 and 208, see Fig. 8) generating a plurality of polarity arrangement control (PAC) signals for a plurality of frames (polarity data signal; see Figs. 4 and 8), each corresponding to a set of aperiodical polarity order; and a PAPDD (a circuitry including elements 205, 206, and 412, see Figs. 8 and 12) receiving the polarity arrangement control signals so as to output a set of aperiodic polarity order to the data lines so that the polarities of the pixels are distributed aperiodically (see Figs. 4 and 7). As shown in Fig. 4, Onaya teaches that when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the first frame opposite to the polarity of the second frame, the polarity of the third frame opposite to the polarity of the fourth frame, and etc., i.e., the polarity of the odd frame opposite to the polarity of the even frame. In other words, Onaya teaches that when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the half (odd) of the frames opposite to the polarity of the other half (even) of the frames, such that the polarity distribution of the one half of the frames is complementary to that of the other half of the frames. It would have been obvious to a person of ordinary skill in the art at the time of the invention

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was made to modify the PATG and the PAPDD of Jeong721, in view of the teaching in the Onoya reference, because this would provide a display device capable of displaying a clear, high definition image in which flicker, vertical striping, and horizontal striping are difficult to be observed by a viewer, as taught by Onoya (see paragraphs 0049 and 0051).

As to claims 2 and 3, Jeong721 teaches the PAPDD comprising a plurality of sampling/hold registers (latch block 300 and level shift lock 400, see Fig. 4), a plurality of digital/analog (D/A) converters (D/A converter block 500, see Fig. 4), a plurality of operational amplifiers (buffer block 600 including a plurality of operational amplifiers, see claims 7 and 8), and a plurality of polarity selectors (a switching block 700 including a plurality of switching circuits corresponding to the claimed selectors, see Fig. 4, col. 6, line 43 through col. 7, line 14). Jeong721 further teaches the output of the sampling/hold registers (300, 400) being connected to the input of the D/A converters (500), the output of the D/A converters (500) being connected to the input of the operational amplifiers (600) so that the polarity selectors select the output signals from the operational amplifiers according to the polarity arrangement control signal (POL-INT), and then output the selected signal to the pixels (see Fig. 4, col. 5, line 60 through col. 7, line 15).

As to claim 4, Jeong721 also teaches the polarities of the signals from the operational amplifiers being either positive or negative (see col. 6, lines 30-42).

As to claim 5, this claim is similar to claim 3 except for the particular location of the polarity selectors. See the rejection to claim 3 above. Accordingly, Jeong721 in view of Onoya discloses all the claimed limitations of claim 5 except for the particular location of the polarity selectors, as presently claimed. However, at the time of the invention was made, it would have

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been obvious to a person of ordinary skill in the art to relocate the polarity selectors between the D/A converters and the operational amplifiers, as presently claimed, since a such modification would have involved a mere change in the location of the component. Applicants have not disclosed that the particular position of the polarity selectors as present claimed solves any stated problem, provides an advantage or is used for any particular purpose. One of ordinary skill in the art, furthermore, would have expected Jeong721's invention to perform equally well with the position of the polarity selectors (700) disposed either as shown in fig. 4 of Jeong721 or as recited in claim 5 because the selector ability to perform its function of selecting is not effected by the location of the polarity selectors. Further, a change in location is generally recognized as being within the level of ordinary skill in the art, see In re Japikse, 86 USPQ 70 (CCPA 1950).

Therefore, it would have been obvious to a person of ordinary skill in this art to modify the invention of Jeong721 in view of Onoya to obtain the invention as specified in claim above.

9. Claims 1-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jeong (US 6,008,801) hereinafter Jeong801, and further in view of Onoya.

As to claims 1 and 8, the claimed invention reads on the Jeong801 reference as follows: Jeong801 discloses a conventional liquid crystal display (LCD) (see Fig. 1) and an associate driving method for controlling the polarity of the LCD panel, the LCD device comprising a LCD panel (a pixel array 170) having a plurality of pixels; a scanning unit (an inherent scanning unit) connected to the display panel by a plurality of scanning lines so that the scanning unit controls the pixels of the display panel via the scanning lines; a polarity arrangement timing generator (PATG) (a circuitry including latch 110 as shown in Fig. 1 and a circuitry for generating a plurality of control signals and polarity signals as shown in Fig. 1) for generating a plurality of

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polarity arrangement control (PAC) signals for a plurality of frames (polarity signals POL; see Figs. 1 and 2), each corresponding to a set of periodical polarity order for a plurality of frames, ; and a polarity arrangement programmable data driver (PAPDD) (a driver including elements 120-160 as shown in Fig. 1) connected to a plurality of data lines and receiving the polarity arrangement control signals (POL, VLREF, VHREF), so as to output a set of polarity order to the data lines (see Figs. 6A-6C). Accordingly, Jeong801 discloses all the claimed limitations of these claims except that Jeong801 does not expressly disclose that the PAPDD outputs a set of **aperiodic** polarity order to the data lines so that the polarities of the pixels are distributed aperiodically; and when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the half of the frames opposite to the polarity of the other half of the frames, such that the polarity distribution of the one half of the frames is complementary to that of the other half of the frames, as presently recited in claims 1 and 8.

However, Onoya discloses a related LCD device comprising a PATG (a circuitry including elements 201, 203, 207 and 208, see Fig. 8) generating a plurality of polarity arrangement control (PAC) signals for a plurality of frames (polarity data signal; see Figs. 4 and 8), each corresponding to a set of aperiodical polarity order; and a PAPDD (a circuitry including elements 205, 206, and 412, see Figs. 8 and 12) receiving the polarity arrangement control signals so as to output a set of aperiodic polarity order to the data lines so that the polarities of the pixels are distributed aperiodically (see Figs. 4 and 7). As shown in Fig. 4, Onaya teaches that when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the first frame opposite to the polarity of the second frame, the polarity of the third frame opposite to the polarity of the fourth frame, and etc., i.e., the polarity of the odd frame

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opposite to the polarity of the even frame. In other words, Onaya teaches that when the display panel displays a plurality frames, the PATG and the PAPDD control the polarity of the half (odd) of the frames opposite to the polarity of the other half (even) of the frames, such that the polarity distribution of the one half of the frames is complementary to that of the other half of the frames. It would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the PATG and the PAPDD of Jeong801, in view of the teaching in the Onoya reference, because this would provide a display device capable of displaying a clear, high definition image in which flicker, vertical striping, and horizontal striping are difficult to be observed by a viewer, as taught by Onoya (see paragraphs 0049 and 0051).

As to claims 2 and 5, Jeong801 teaches the PAPDD comprising a plurality of sampling/hold registers (latches 130, 140, see Fig. 1); a plurality of digital/analog (D/A) converters (a plurality of low voltage D/A converters 151 and a plurality of high voltage D/A converter 152, see Fig. 2, col. 1, line 65 through col. 12); a plurality of polarity selectors (a plurality of multiplexors 153, see Fig. 2, col. 2, lines 13-22); and an output buffer block (180) (see Fig. 1). Jeong801 further teaches the output buffer block including a plurality of operational amplifiers (plural buffers including plural operational amplifiers OP3 as shown in Fig. 11, col. 8, lines 26-35). Jeong further teaches the output of the sampling/hold registers (130, 140) being connected to the input of the D/A converters (151, 152), the output of the D/A converters (151, 152) being connected to the input of the polarity selectors (153) so that the polarity selectors select the output signals from the D/A converters (151, 152) according to the polarity arrangement control signals (POL, VLREF, VHREF), and then output the selected signal to the data lines through the operational amplifiers (OP3) (see Figs. 1, 1 and 11).

As to claim 3, this claim is similar to claim 5 except for the particular location of the polarity selectors. See the rejection to claim 5 above. Accordingly, Jeong801 in view of Onoya discloses all the claimed limitations of claim 3 except for the particular location of the polarity selectors, as presently claimed. However, at the time of the invention was made, it would have been obvious to a person of ordinary skill in the art to relocate the polarity selectors following the operational amplifiers, as presently claimed, since a such modification would have involved a mere change in the location of the component. Applicants have not disclosed that the particular position of the polarity selectors as present claimed solves any stated problem, provides an advantage or is used for any particular purpose. One of ordinary skill in the art, furthermore, would have expected Jeong801's invention to perform equally well with the position of the polarity selectors (153) disposed either as shown in fig. 2 of Jeong801 or as recited in claim 3 because the selector ability to perform its function of selecting is not effected by the location of the polarity selectors. Further, a change in location is generally recognized as being within the level of ordinary skill in the art, see **In re Japikse, 86 USPQ 70 (CCPA 1950)**. Therefore, it would have been obvious to a person of ordinary skill in this art to modify the invention of Jeong801 in view of Onoya to obtain the invention as specified in claim above.

As to claim 4, Jeong801 also teaches the polarities of the signals from the operational amplifiers being either positive or negative (see Fig. 2, col. 2, lines 13-22).

Response to Arguments

10. Applicant's arguments filed 1/23/2007 have been fully considered but they are not persuasive.

With respect to the rejections under 35 USC 102(b) to claims 1, 2 and 8 as being anticipated by Onoya, in the Office Action dated 10/23/2006, Applicants argue that Onoya fails to teach (i) “predefined control signals” and (ii) “distribution of the entire polarities of the frames in complementary and neutralized to zero in total, so as to reduce crosstalk and enhance image quality”, see page 5 of the amendment. With respect to the first distinction (i), Examiner disagrees because Fig. 4 shows a first PAC signal for a first frame period to cause a first set of aperiodical polarity order “+---+---+---+---”, i.e., a first PAC signal is predefined to cause the first set of aperiodical polarity order happened in, a second PAC signal for a second frame period to cause a second set of aperiodical polarity order “-+--+-+--+-+--”, which is opposite to the polarity of the first set of aperiodical polarity order, i.e., a second PAC signal is predefined to cause the second set of aperiodical polarity order happened, and so on. With respect to the second distinction (ii), Examiner disagrees because (1) at least the independent claims 1 and 8 do not presently recite “distribution of the entire polarities of the frames ... **neutralized to zero in total, so as to reduce crosstalk and enhance image quality**”, as argued by Applicants (Note that the specification is not the measure of invention. Therefore, limitations contained therein can’t be read into the claims for the purpose of avoiding the prior art. See *In re Sporek*, 55 CCPA 743, 386 F.2d 924, 155 USPQ 687 (1968)), (2) “the polarity distribution of the one half of the frames being complementary to that of the other half of the frames” does not imply a number of **negative** polarities equal to a number of **positive** polarities, e.g., a complement angle of a 60-degree angle is a 30-degree angle, but not a 60-degree angle (see Merriam Webster’s Collegiate Dictionary, tenth Edition), and (3) note that Fig. 4 just shows the first five frame period and the polarity distribution of the six frame period is opposite to that of the fifth frame period in the

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same manner as the first and second frame periods and as the third and fourth frame periods. In other words, the entire polarities of all the frames are neutralized to zero.

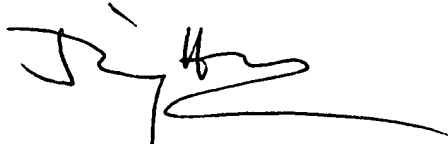
Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Thursday, 7:00 a.m. - 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
February 2, 2007



Jimmy H. Nguyen
Primary Examiner
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